WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a first semiconductor memory having a first peripheral circuit which transmits and receives memory data to/from a first memory cell array;

a second semiconductor memory having a second peripheral circuit which transmits and receives the memory data to/from a second memory cell array; and

a part of the peripheral circuit of the first semiconductor memory formed adjacent to the second memory cell array by a design rule of the second peripheral circuit.